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ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/410,160	BELL ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 9/30/99 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION-NonFinal

Examined

1. **Claims 1-13 have been submitted, examined, and rejected.**

Drawings-draftperson objection

This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed. Specifically, see the enclosed Form 948, Notice of Draftperson's Drawing Patent Review which objects to the drawings.

Specification-objections-informalities

2. **The disclosure is objected to because of the following informalities.** Appropriate correction is required.
3. Page 5, line 1 states "References to "verilog" refer **generally** to the verilog hardware description language (HDL) as defined by the IEEE 1364-1995 standard." The Examiner suggests that the word "generally" be deleted from this sentence. If "generally" is not deleted, then the Examiner requests an explanation of what else "verilog" refers to.

Drawings-"alternate block diagrams"

4. The specification Page 4 line 7 states "FIG. 2 is an alternate block diagram of the present invention." It is unclear if FIG 2 represents the same preferred embodiment displayed in FIG 1, or if FIG 2 is a block diagram of a different or alternate embodiment.
5. Similarly, the specification Page 9 line 9 states "FIG 3. is another alternate block diagram of the present invention". Again, it is unclear if FIG 3 represents the same preferred

embodiment displayed in FIG 1, or if FIG 3 is a block diagram of a different or alternate embodiment.

6. The Examiner requests that the drawings be described or drawn in a way to specify if they represent different embodiments, or they represent the same embodiment.
7. For purposes of examination, the Examiner will treat these figures as referring to the same preferred embodiment.

Drawings-reference characters

8. The drawings of this application improperly use reference characters. "The same part of an invention appearing in more than one view of the drawing must always be designated by the same reference character, and the same reference character must never be used to designate different parts" according to 37 CFR 1.84(p)(4).
9. Specifically, Page 9 line 10 states "repair block 120", in contradiction to FIG 1 element 120 which states "repair program". The Examiner requests that this inconsistency be corrected.

Claim Rejections - 35 USC § 112- first paragraph- description

10. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

11. **Claims 7-11 are rejected under 35 U.S.C. 112, first paragraph**, as containing subject matter which was not described in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

12. **Claim 7 is rejected** under 35 U.S.C. 112, first paragraph because it contains the phrase **"repair file".** The specification does not describe "repair file". "Repair block" is described at specification Page 9 lines 10-19. This description includes the word "may" six separate times, and is very unclear. Additionally, "repair memo" is described at specification Page 11 lines 2-5, and this description includes the word "may" four separate times.
13. Thus, there is no description of the claimed limitation phrase "repair file", but there are unclear descriptions of "repair block" and of "repair memo" containing the word "may" a total of ten times.
14. The meaning of the word "may" is very problematic in this context. It is unclear if the Applicant is describing an invention that has the simultaneous capacity to perform all of these features, or if Applicant is describing an invention that can perform at least one of these features. Or perhaps an invention that does not perform any of these features.
15. Thus, Claim 7 is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.
16. **Claim 8 is rejected** under 35 U.S.C. 112, first paragraph. Claim 8 depends from Claim 7, inherits the same defect, and is rejected for the same reasons. Additionally, the Claim 8 phrase **"laser repair program"** is not described in the specification.

17. **Claim 9 is rejected** under 35 U.S.C. 112, first paragraph because it contains the phrase **"repair program".** "Repair program" is shown in FIG 1 element 120, and mentioned in FIG 3 elements 306 and 318. Note that FIG 1 element 120 is called "repair block 120" at specification Page 9 line 10.

18. Thus, it is unclear if the phrase "repair program" in the claim refers to "repair block" as described at specification Page 9 lines 10-19. Even if the Examiner assumes that "repair program" equals "repair block", this written description (Page 9 lines 10-19) of "repair block 120" includes the word "may" six separate times, and is very unclear. The meaning of the word "may" is very problematic in this context. It is unclear if the Applicant is describing an invention that has the simultaneous capacity to perform all of these features, or if Applicant is describing an invention that can perform at least one of these features. Or perhaps an invention that does not perform any of these features.

19. Additionally, there is no description of how to simulate this repair program.

20. Thus, Claim 9 is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

21. **Claim 10 is rejected** under 35 U.S.C. 112, first paragraph because it contains the phrase **"repair program".** Claim 10 is rejected for the same reasons as Claim 9 above.

22. **Claim 11 is rejected** under 35 U.S.C. 112, first paragraph. Claim 11 depends from Claim 10, inherits the same defect, and is rejected for the same reasons as Claim 10

Claim Rejections - 35 USC § 112-Second Paragraph-indefinite

23. The following is a quotation of the second paragraph of 35 U.S.C. 112:

24. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

25. **Claims 7-11 are rejected under 35 U.S.C. 112, second paragraph,** as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

26. **Claim 7 is rejected** under 35 U.S.C. 112, second paragraph because the phrase **"repair file"** is indefinite. "Repair block" is defined at specification Page 9 lines 10-19. This definition includes the word "may" six separate times, and is very unclear. Additionally, "repair memo" is defined at specification Page 11 lines 2-5, and this definition includes the word "may" four separate times.

27. Thus, there is no definition of the claimed limitation phrase "repair file", but there are unclear definitions of "repair block" and of "repair memo" containing the word "may" a total of ten times.

28. The meaning of the word "may" is very problematic and ambiguous in this context. It is unclear if the Applicant is describing an invention that has the simultaneous capacity to perform all of these features, or if Applicant is defining an invention that can perform at least one of these features.

29. **Claim 8 is rejected** under 35 U.S.C. 112, second paragraph. Claim 8 depends from Claim 7, inherits the same defect, and is rejected for the same reasons. Additionally, the Claim 8 phrase **"laser repair program"** is not adequately defined in the specification.

30. **Claim 9 is rejected** under 35 U.S.C. 112, second paragraph because it contains the phrase **"repair program"** is indefinite. "Repair program" is shown in FIG 1 element 120, and mentioned in FIG 3 elements 306 and 318. FIG 1 element 120 is called "repair

block 120". Thus, it is unclear if the phrase "repair program" in the claim refers to "repair block" as described at specification Page 9 lines 10-19. Even if the Examiner assumes that "repair program" equals "repair block", this written description of "repair block" includes the word "may" six separate times, and is very unclear. The meaning of the word "may" is very problematic and ambiguous in this context. It is unclear if the Applicant is describing an invention that has the simultaneous capacity to perform all of these features, or if Applicant is defining an invention that can perform at least one of these features. Or an invention that does not perform any of these features.

31. Thus, Claim 9 is not adequately defined.

32. **Claim 10 is rejected** under 35 U.S.C. 112, first paragraph because it contains the phrase **"repair program".** Claim 10 is rejected for the same reasons as Claim 9 above.

33. **Claim 11 is rejected** under 35 U.S.C. 112, first paragraph. Claim 11 depends from Claim 10, inherits the same defect, and is rejected for the same reasons.

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34. **Sample** refers to Sample et al. US Patent 5,841,967 filed 10/17/96, issued 11/24/98.

35. **Tzori** refers to Tzori US Patent 6,202,044 B1 filed 6/12/98, issued 3/13/01.

36. **Higgins** refers to Higgins et al. US Patent 6,397,349 B2 filed 10/13/98, issued 5/28/02.

Claim Interpretation

37. The phrase "and/or" is used in many of the claims. The Examiner interprets "and/or" as meaning a logically inclusive "or" (in a Boolean logic sense, and in contrast to the logically exclusive "or"). In other words, A and/or B is interpreted to mean one of the following three possibilities: {A, B, (A and B)}.

Claim Rejections - 35 USC § 102(e)

38. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

39. A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

40. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

41. **Claims 1, 4, 5, 6, 12, and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Sample.**

42. **Claim 1 is rejected** under 35 U.S.C. 102(e) as being anticipated by Sample. Claim 1 is an independent claim with two limitations.

43. **A-"enumeration of a plurality of fuses"** is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE". Also, note Column 1 lines 38-46 "The next design stage transforms the netlist of gates and flip-flops into a transistor list or layout. Thus, gates and flip-flops are replaced with their transistor equivalents or library cells. During the cell and transistor selection process, timing and loading requirements are taken into consideration. Finally, the design is manufactured,

whereby the transistor list or layout specification is used to bum [sic] fuses of a programmable device or to generate masks for integrated circuit fabrication."

44. **B-"compiling data for each one of said plurality of fuses...schematic path data...[or] simulation path data...[or] physical location data"** is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE". Also, note Column 1 lines 38-46 "The next design stage transforms the netlist of gates and flip-flops into a transistor list or layout. Thus, gates and flip-flops are replaced with their transistor equivalents or library cells. During the cell and transistor selection process, timing and loading requirements are taken into consideration. Finally, the design is manufactured, whereby the transistor list or layout specification is used to bum [sic] fuses of a programmable device or to generate masks for integrated circuit fabrication."
45. **Claim 4 is rejected** under 35 U.S.C. 102(e) as being anticipated by Sample. Claim 4 depends from Claim 1 with one new limitation.
46. **"step (B) further comprises the sub-step of: generating a list of layout coordinates and schematic instance paths as part of said compiling"** is disclosed by Sample at FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE".
47. **Claim 5 is rejected** under 35 U.S.C. 102(e) as being anticipated by Sample. Claim 5 depends from Claim 1 with one new limitation.
48. **"comprising one or more fuse reports"** is disclosed by Sample at Column 1 lines 38-46 "The next design stage transforms the netlist of gates and flip-flops into a transistor list or layout. Thus, gates and flip-flops are replaced with their transistor equivalents or library

cells. During the cell and transistor selection process, timing and loading requirements are taken into consideration. Finally, the design is manufactured, whereby the transistor **list** or layout specification **is used to bum [sic] fuses** of a programmable device or to generate masks for integrated circuit fabrication." Note that burning the fuses inherently requires a "fuse report" identifying which fuses should be burned.

49. **Claim 6 is rejected** under 35 U.S.C. 102(e) as being anticipated by Sample. Claim 6 depends from Claim 5 with one new limitation.

50. **"listing physical location of one or more devices in response to said fuse reports"** is disclosed by Sample at Column 1 lines 43-46 "Finally, the design is manufactured, whereby the transistor list or **layout specification is used to bum [sic] fuses** of a programmable device or to generate masks for integrated circuit fabrication." Note that burning the fuses requires listing the physical location of the fuses to be burned, so that a high (burning) voltage can be applied across those locations. Also, note FIG 13 element 148 "PART, PLACE, ROUTE".

51. **Claim 12 is rejected** under 35 U.S.C. 102(e) as being anticipated by Sample. Claim 12 is an **"apparatus" claim** with the same limitations as Claim 1, and thus is rejected for the same reasons.

52. **Claim 13 is rejected** under 35 U.S.C. 102(e) as being anticipated by Sample. Claim 13 is an **"apparatus" claim** with "means for" language and with the same limitations as Claim 1, and thus is rejected for the same reasons.

Claim Rejections - 35 USC § 103

53. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

54. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

55. **Claims 2, 3, 7-11 are rejected under 35 U.S.C. 103(a) as unpatentable.**

56. **Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sample in view of Tzori**. Claim 2 depends from Claim 1 with one new limitation.

57. Sample does not expressly disclose "simulation path data comprises verilog simulation path data".

58. **"simulation path data comprises verilog simulation path data"** is disclosed by Tzori at Column 1 line 28 "Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making

up a Verilog model include modules for each digital logic circuit included in the simulation, for **specifying interconnections among the Verilog logic circuit modules**".

59. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori to modify Sample. One of ordinary skill in the art would have been motivated to do this to "Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype" according to Tzori Column 1 line 41.

60. **Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sample in view of Tzori**. Claim 3 depends from Claim 1 with one new limitation.

61. Sample does not expressly disclose "said schematic path data comprises schematic paths, properties, hierarchy [or] verilog paths".

62. **"said schematic path data comprises schematic paths, properties, hierarchy and/or verilog paths"** is disclosed by Tzori at Column 1 line 28 "Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for **specifying interconnections among the Verilog logic circuit modules**".

63. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori to modify Sample. One of ordinary skill in the art would have been motivated to do this to "Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype" according to Tzori Column 1 line 41.

64. **Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sample in view of Tzori, and further in view of Higgins**. Claim 7 depends from Claim 1 with one new limitation.

65. "repair file" is interpreted by the Examiner as referring to "repair memo" as described in Page 11 line 2 of the specification. Note that this phrase has been rejected as indefinite. However, in the interests of compact prosecution:

66. **"repair file"** is disclosed by Higgins Column 1 line 58 "a table listing faulty addresses".

67. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Higgins to modify Sample. One of ordinary skill in the art would have been motivated to do this to "Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype" according to Tzori Column 1 line 41, and because "repair procedures result in higher yields" according to Higgins Column 1 line 24.

68. **Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sample in view of Tzori, and further in view of Higgins**. Claim 8 depends from Claim 7 with one new limitation.

69. "laser repair program" is not described in the specification, and this claim has been rejected above for indefiniteness.

70. **"laser repair program"** is disclosed by Higgins Column 1 line 20 "Location information is then supplied to a controller for a laser repair device, which achieves a hardware fix."

71. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Higgins to modify Sample. One of ordinary skill in the art

would have been motivated to do this to "Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype" according to Tzori Column 1 line 41, and because "repair procedures result in higher yields" according to Higgins Column 1 line 24.

72. **Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sample in view of Tzori.** Claim 9 depends from Claim 1 with one new limitation.

73. **"verifying a function of a repair program with one or more simulations"** is disclosed by Tzori at Column 1 line 17 "Various different software and hardware systems exist for simulating and/or emulating".

74. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori to modify Sample. One of ordinary skill in the art would have been motivated to do this to "Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype" according to Tzori Column 1 line 41.

75. **Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sample in view of Tzori.** Claim 9 depends from Claim 1 with one new limitation.

76. **"list of coordinates of fuses that need to be blown for the desired repair"** is disclosed by Sample Column 1 line 44 "list or layout specification is used to bum [sic] fuses".

77. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tzori and Higgins to modify Sample. One of ordinary skill in the art would have been motivated to do this to "Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype" according to Tzori Column 1

line 41, and because "repair procedures result in higher yields" according to Higgins Column 1 line 24.

78. **Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sample in view of Tzori.** Claim 11 depends from Claim 10 with one new limitation.

79. **"storing said coordinates in a memory"** is disclosed by is disclosed by Sample Column 1 line 44 "list or layout specification is used to bum [sic] fuses". Note that said list inherently has the coordinates necessary to locate and burn the fuse, and that in modern manufacturing systems said list would inherently be stored in a memory.

Conclusion

80. The following documents are also cited as prior art. The Applicant should review these documents carefully before replying.

81. **Maeda US Patent 5,568,408 Abstract discloses "automatically carry out a repair work on the defective semiconductor memories", and FIG 11 discloses "REPAIR DATA FILE.**

82. Rodriguez US Patent 5,821,160 Abstract discloses "fuse region" and "laser access and repair".

83. Mifsud US Patent 6,081,910 Abstract discloses "two-pass fuse blow".

84. Brown US Patent 4,658,400 Abstract discloses "location of faulty elements...stores these location".

85. Massoumi US Patent 6,115,300 Column 5 line 15 "electrical fuse interconnect, laser or other equivalent programming repair scheme.

86. Handa US Patent 6,067,259 Abstract discloses "repairing faulty elements of first memory cells"

87. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 7:00 PM.

88. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are:

89. (703) 746-7238 --- for communications after a Final Rejection has been made;

90. (703) 746-7239 --- for other official communications; and

91. (703) 746-7240 --- for non-official or draft communications.

92. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * *

William Thomson
Patent Examiner
A.U. 2123